Claims

[c1] What is claimed is:

1.A method for making a microdisplay pixel cell, the method comprising:

providing a semiconductor substrate defined with a plurality of active areas;

forming a gate oxide layer and a gate conductive layer sequentially on the semiconductor substrate;

performing a photo-etching-process(PEP) to the gate conductive layer to form at least one gate on the semiconductor substrate and the gate covering a portion of the active area;

forming a plurality of source/drain(S/D) in the active area not covered by the gate;

forming a first dielectric layer on the semiconductor substrate to cover the gate and the source/drain;

forming at least one row select contact plug in the first dielectric layer to electrically connect to the gate;

forming at least one row select line atop the first dielectric layer, the row select line being electrically connected to the gate through the row select contact plug;

forming a second dielectric layer atop the first dielectric layer and covering the row select line;

forming at least one pixel cap top plate atop the second dielectric layer;

forming a capacitor dielectric layer atop the surface of the top plate; and

forming at least one pixel cap bottom plate atop the second dielectric layer and covering the top plate.

[c2] 2.The method of claim 1 wherein the gate conductive layer is a polysilicon layer.

[c3] 3. The method of claim 1 wherein at least one first contact plug is formed in the first dielectric layer and the second dielectric layer for electrically connecting the source and the top plate.

[c4] 4.The method of claim 1 wherein at least one second contact plug is formed in the first dielectric layer and the second dielectric layer for electrically connecting the drain to a video data line.

[c5] 5.The method of claim 1 wherein the row select line is composed of a metal and

is used as a scan line of the microdisplay.

[c6] 6.The method of claim 1 wherein both the bottom plate and the top plate are composed of a metal.

[c7] 7.The method of claim 6 wherein the metal forming the bottom plate and the top plate comprises titanium (Ti), titanium nitride (TiN), aluminum (Al), copper (Cu) or an alloy of above-mentioned materials.

[c8] 8.The method of claim 1 wherein the pixel cell comprises two gates, two common drains, four sources, four top plates and one bottom plate stacking in sequence from bottom to top.

[c9] 9.The method of claim 1 wherein the microdisplay is a reflective liquid crystal on silicon (LCOS) display.

[c10] 10.A method for making a microdisplay pixel cell, the method comprising:
providing a semiconductor substrate defined with a plurality of active areas;
forming at least one gate on the semiconductor substrate and the gate covering a portion of the active area;
forming a plurality of source/drain(S/D) in the active area not covered by the gate;
forming a first dielectric layer on the semiconductor substrate to cover the gate and the source/drain;
forming at least one pixel cap top plate atop the first dielectric layer;
forming a capacitor dielectric layer atop the surface of the top plate; and
forming at least one pixel cap bottom plate atop the first dielectric layer and covering the top plate.

[c11] 11.The method of claim 10 wherein a method for forming the gate comprises:
forming a gate oxide layer and a polysilicon layer sequentially on the semiconductor substrate; and
performing a photo-etching-process(PEP) to the polysilicon layer to simultaneously form at least one gate and at least one row select line electrically connected to the gate on the semiconductor substrate, the gate covering a portion of the active area.

[c12] 12.The method of claim 10 further comprises forming a second dielectric layer under the first dielectric layer and the second dielectric layer covers the gate and the source/drain.

[c13] 13.The method of claim 12 further comprises the following steps:
forming at least one row select contact plug electrically connected to the gate in the second dielectric layer;
forming at least one row select line atop the second dielectric layer, the row select line being electrically connected to the gate through the row select contact plug; and
forming the first dielectric layer to cover the row select line.

[c14] 14.The method of claim 13 wherein the row select line is composed of a metal and is used as a scan line of the microdispaly.

[c15] 15.The method of claim 10 wherein both the bottom plate and the top plate are composed of metal and the metal material comprises titanium (Ti), titanium nitride (TiN), aluminum (Al), copper (Cu) or an alloy of above-mentioned materials.

[c16] 16.The method of claim 10 further comprises forming at least one first contact plug in the first dielectric layer and the second dielectric layer for electrically connecting the source and the top plate.

[c17] 17.The method of claim 10 further comprises forming at least one second contact plug in the first dielectric layer and the second dielectric layer for electrically connecting the drain to a video data line.

[c18] 18.The method of claim 10 wherein the pixel cell comprises two gates, two common drains, four sources, four top plates and one bottom plate stacking in sequence from bottom to top.

[c19] 19.The method of claim 10 wherein the microdisplay is a reflective liquid crystal on silicon (LCOS) display.

[c20] 20.A microdisplay pixel cell device, the device comprising:
a semiconductor substrate defined with a plurality of active areas;

at least one gate, the gate covering a portion of the active area;
at least one source/drain(S/D), the source/drain being in the active area not covered by the gate;
a first dielectric layer, the first dielectric layer covering the gate and the source/drain, the first dielectric layer comprising at least one row select contact plug to electrically connect to the gate;
at least one row select line, the row select line being atop the first dielectric layer, the row select line being electrically connected to the gate through the row select contact plug;
a second dielectric layer, the second dielectric layer being atop the first dielectric layer and covering the row select line;
at least one pixel cap top plate, the pixel cap top plate being atop the second dielectric layer;
at least one capacitor dielectric layer, the capacitor dielectric layer being atop the surface of the top plate; and
at least one pixel cap bottom plate, the pixel cap bottom plate being atop the second dielectric layer and covering the top plate and the capacitor dielectric layer.

[c21] 21.The device of claim 20 wherein the gate comprises a gate oxide layer, a polysilicon layer or a metal silicide layer.

[c22] 22.The device of claim 20 wherein at least one first contact plug is comprised in the first dielectric layer and the second dielectric layer for electrically connecting the source and the top plate.

[c23] 23.The device of claim 20 wherein at least one second contact plug is comprised in the first dielectric layer and the second dielectric layer for electrically connecting the drain to a video data line.

[c24] 24.The device of claim 20 wherein the row select line is composed of a metal and is used as a scan line of the microdisplay.

[c25] 25.The device of claim 20 wherein both the bottom plate and the top plate are composed of a metal.

[c26] 26.The device of claim 25 wherein both the bottom plate and the top plate are composed of titanium (Ti), titanium nitride (TiN), aluminum (Al), copper (Cu) or an alloy of above-mentioned materials.

[c27] 27.The device of claim 20 wherein the pixel cell comprises two gates, two common drains, four sources, four top plates and one bottom plate stacking in sequence from bottom to top.

[c28] 28.The device of claim 20 wherein the microdisplay is a reflective liquid crystal on silicon (LCOS) display.